The degradation of poly-Si thin film transistors (TFTs) under self-heating stress was investigated via the capacitance between the source and the gate ($C_{GS}$), and that between the drain and the gate ($C_{GD}$). Consequently, the normalized $C_{GS}$ and $C_{GD}$ after stress positively shift 2 V for the gate voltage near flat band voltage. In addition, $C_{GS}$ raises about 40% for the lower gate voltage, while $C_{GD}$ raises only about 10%. With simulation results, it is found that the self-heating effect creates interface states near the source region and the deep states near drain, resulting in the different inclines of the of $C_{GS}$ and $C_{GD}$ curves.

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**Experimental**

The process flow of TFTs is described below. First, the buffer oxide and a 50 nm thick a-Si:H film were deposited on glass substrates with PECVD. The samples were then put into the oven for dehydrogenation. The XeCl excimer laser of wavelength 308 nm and energy density of 400 mJ/cm² was applied. The laser scanned the a-Si:H film with the beam width of 4 mm and 98% overlap to recrystallize the a-Si:H film to poly-Si. After poly-Si active area definition, 100 nm SiO₂ was deposited with plasma-enhanced chemical vapor deposition (PECVD) as the gate insulator. Next, the metal gate was formed by sputter and then defined. The lightly doped drain (LDD) and the n⁺ source/drain doping were formed by PH₃ implantation with dosage $2 \times 10^{13}$ and $2 \times 10^{15}$ cm⁻² of PH₃ respectively. The LDD implantation was self-aligned and the n⁺ regions were defined with a separate mask. Then, the interlayer of SiN was deposited. Subsequently, the rapid thermal annealing was conducted to activate the dopants. Meanwhile, the poly-si film was hydrogenated. Finally, the contact hole formation and metallization were performed to complete the fabrication work.

In this study, the n-type TFTs with a channel width of 20 μm and a channel length of 5 μm with an LDD structure of length 1.2 μm are fabricated. These devices are stressed with a self-heating condition, that is, the gate to source voltage $Vgs$ and the drain to source voltage $Vds$ are both 18 V. The C-V curves of the gate-to-source capacitance ($C_{GS}$) and gate-to-drain capacitance ($C_{GD}$) before and after stress with different frequencies are measured with the Agilent 4284A precision LCR meter.

**Results and Discussion**

Figure 1 shows the capacitance-voltage (C-V) transfer curves of the poly-Si TFTs after self-heating stress with the time duration of 500 s. The higher threshold voltage, lower on-current, and smaller sub-threshold slope are observed. Uraoka et al. previously reported that the self-heating effect causes the release of hydrogen in the poly-Si film and therefore increases the deep states, resulting in the degradation of sub-threshold region of the I-V transfer characteristics. However, Fuyuki et al. also reported that the degradation from self-heating may not only increase the trap states in the poly-Si film but also raise the interface states between poly-Si film and gate oxide, as well as the trap charges in the oxide.

Because the I-V transfer characteristics could not distinguish the dominant degradation mechanism, capacitance-voltage (C-V) measurements were employed. Figure 2a shows the normalized gate-to-source capacitance $C_{GS}$ curves before and after stress with different frequencies, while Fig. 2b shows the corresponding curves of the normalized gate-to-drain capacitance $C_{GD}$. The $C_{GS}$ is measured with a floating drain and $C_{GD}$ is measured with a floating source. The normalized capacitance is the ratio of the measured capacitance to a constant of 40 fF, which is the gate oxide capacitance of the TFT under test. As shown in Fig. 2a, the normalized $C_{GS}$ curves significantly stretch out and shift in the positive direction after stress. In addition, the capacitance of the device after stress increases dramatically as the gate voltage is smaller than the flatband voltage ($V_{FB}$). Similar degradation behavior may also be observed in the normalized $C_{GD}$ curves, as shown in Fig. 2b. For the curves of $C_{GS}$ and $C_{GD}$ after self-heating stress, the stretch and shift in the positive direction for the gate voltage near $V_{FB}$ can be explained by the increase of the deep states during stress. However, the additional increase of the capacitance below $V_{FB}$ and the different degrees of the increases in $C_{GS}$ and $C_{GD}$ suggest that there may be another mechanism in the device during self-heating stress, which implies the inference from Fuyuki.

The increases of the $C_{GS}$ and $C_{GD}$ curves for the gate voltage smaller than $V_{FB}$ may come from the interface states near source and the trapped charge in the gate insulator. Nevertheless, it is observed that both $C_{GS}$ and $C_{GD}$ curves for the stressed devices shift in the positive direction at the higher frequency. Because the trapped charges in the gate insulator would not respond to different frequencies, the increases of the $C_{GS}$ and $C_{GD}$ curves for the lower gate voltage may be attributed to the interface states. Moreover, the more apparent increase of $C_{GS}$ below $V_{FB}$ than the one of $C_{GD}$ may also be attributed to the interface states induced by the higher local electric field between the gate and the source than that between the gate and the drain. It hints of a spatial creation of interfacial states according to the electric field distribution. Furthermore, it is reported that the temperature increase due to the self-heating stress near the drain is higher than that near the source and exhibits a spatial distribution. Because the high temperature in the poly-Si film will release hydrogen and increase the deep states, it may be expected that the increase of deep states near the drain will be more obvious. Therefore, a device under self-heating stress is expected to suffer the temperature effect near the drain, and the high electric field near the source.

To verify the hypothesis about the damaged regions, a two-
dimensional (2-D) numerical simulation program DESSIS was used to simulate the device characteristics. The model of the cross section of the device after self-heating stress is shown in Fig. 3. In the simulation, the grain boundaries inside the poly-Si film are accounted by using the “effective medium approach,” which treats the poly-Si film as a uniform material with the density of localized states in the forbidden gap. The deep states are arranged to be gradually decreasing from drain to source according to the temperature distribution under self-heating conditions. The deep states in the poly-Si film are modeled by a Gaussian distribution near the mid-gap. The peak value of the deep state density changes from $5 \times 10^{18}$ to $3 \times 10^{17}$ cm$^{-3}$ in the range of 0.3 $\mu$m at the drain edge, corresponding to the temperature distribution. On the other hand, the interface states of $1 \times 10^{15}$ cm$^{-2}$ decreasing to $1 \times 10^{14}$ cm$^{-2}$ are arranged from the source edge, reflecting the electric field between the gate and source. Figure 4 shows the simulation results with different degraded regions in the device. Curve A is the C-V curve with no degraded region, while curve B is the one only with interface states near the source region. Compared to curve A, curve B increases drastically for the gate voltage below $V_{FB}$. This reveals that the interface states between the source and the gate influence the induced carriers in channel depletion and weak inversion conditions.

Although the effective medium approach is used in this simulation, the generated surface states may come from the grain boundaries of the poly-Si film near source region. Curve C further includes the increase of deep states in the poly-Si film near the drain. It can be seen that the capacitance not only increases below $V_{FB}$ but also shifts in the positive direction for the gate voltage near $V_{FB}$. Thus, the shift of curve C near $V_{FB}$ is attributed to more deep states to be filled during weak and strong inversion. The similarity of Curve C and the measured $C_{GS}$ and $C_{GD}$ indicates that the degradation due to
self heating stress causes the increases of deep states in the poly-Si film and the interface states near the source. This finding via the C-V measurements may be important for the further comprehension of the degradation caused by self-heating stress.

Conclusions

In this work, the degradation of poly-Si TFTs under self-heating stress is examined via employing C-V measurement. It was found that the degradation contains not only the increase of the deep states inside the poly-Si film but also the increase of interface states between the poly-Si film and the gate insulator, owing to the high voltage difference between gate and source. The increase of these states will result in the increase of the capacitance for the gate voltage less than $V_{FB}$ and the shift in the positive direction for the gate voltage about $V_{FB}$. The degradation of C-V characteristics is quite important in circuit applications such as the ring oscillators and dynamic shift registers because these circuits are sensitive to the capacitance values of the transistors. This understanding of the degradation mechanisms of self-heating effect on the I-V and C-V characteristics will be helpful in realizing system on panel design.

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