Flat band voltage control on low $V_t$ metal-gate/high-$\kappa$ CMOSFETs with small EOT (Invited Paper)

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The unwanted high threshold voltage ($V_t$) is the major challenge for metal-gate/high-$\kappa$ CMOS especially at small equivalent-oxide-thickness (EOT). We have investigated the high $V_t$ issue that is due to flat-band voltage ($V_{fb}$) roll-off at smaller EOT. A mechanism of charged oxygen vacancies formed by interface reaction was proposed to explain the $V_{fb}$ roll-off effect. This interface reaction can be decreased by inserting a thin interfacial SiON and using novel low temperature process. The self-aligned and gate-first metal-gate/high-$\kappa$ CMOSFETs using these methods have achieved low $V_t$ and good control of $V_{fb}$ roll-off at small 0.6–1.2 nm EOT.

1. Introduction

After nearly a decade long research, high-$\kappa$ gate dielectric [1–16] has been used for 45 nm node CMOS [13] and below [16]. This technology is mandatory to decrease the gate leakage current and DC power consumption in VLSI ICs. However, the metal-gate/high-$\kappa$ CMOS still has difficult challenges, which are to scale down the equivalent-oxide thickness (EOT) and lower down the undesired high threshold voltage ($V_t$). The unwanted high $V_t$ is related to the Fermi-level pinning effect in HfO$_2$-based high-$\kappa$ gate dielectric, which shifts the effective work-function of metal-gate from band edge toward mid-gap [7,8], although the detailed mechanism is still under investigation. Nevertheless, continuously lower down the $V_t$ to a minimum $4kT/q$ value is the scaling trend for high performance low voltage ICs [17].

The unwanted high $V_t$ issue is especially hard for p-MOS. This is because only Ir and Pt in the Periodic Table have the needed high work-function larger than the target 5.2 eV of Si valance band [9]. Unfortunately, both Ir and Pt are not thermally stable on thin high-$\kappa$ gate dielectric [9]. Furthermore, the flat band voltage ($V_{fb}$) roll-off effect at smaller EOT [11,14] further worsens the required low $V_t$ challenge. These tough challenges are evident from the slower EOT scaling: the using 1.0 nm EOT of Intel’s 1st-generation high-$\kappa$ + metal-gate CMOS for 45 nm node to only 0.9 nm EOT of 2nd-generation technology for 32 nm node [16].

To address these issues, in this paper we present a possible mechanism of $V_{fb}$ roll-off effect at smaller EOT – the charged oxygen vacancies generated by interface reaction. Based on the proposed mechanism, we have developed a low temperature process for metal-gate/high-$\kappa$ CMOS using laser-reflective-gate MOS structure [15] or silicide-induced doping for source–drain shallow junction [14]. The fabricated metal-gate/high-$\kappa$ CMOSFETs using above methods have good control of $V_{fb}$ roll-off with low $V_t$ values at small 0.6–1.2 nm EOT, with several orders of magnitude lower gate leakage than poly-Si/SiO$_2$ stack at the same EOT. Such good transistor performance further supports our proposed mechanism of $V_{fb}$ roll-off effect.

2. Experimental procedure

Standard Si wafers with ~10 ohm cm resistivity were used in this study. To address the Fermi-level pinning effect in HfO$_2$-based high-$\kappa$ gate dielectrics [7,8], we added our pioneered La$_2$O$_3$ [4] and
Al₂O₃ [12] in HfO₂ [3], which have unique negative [4,5] and positive Vfb for n- and p-MOSFETs, respectively. After depositing the different high-κ gate dielectrics on Si substrate using physical vapor deposition (PVD), a post-deposition anneal (PDA) under O₂ is applied to decrease the defects in gate dielectric. To improve the interface reaction and mobility, some transistors have a thin SiON layer inserted in the high-κ and Si interface. Various SiON thicknesses of 0.8–1.5 nm have been studied to optimize the EOT and interface reaction. After depositing different work-function metal-gates on high-κ dielectric using PVD and subsequent gate patterning, a self-aligned ion implantation was performed for source–drain doping and followed by 1000 °C rapid-thermal annealing (RTA) or excimer laser annealing. Here the scanned KrF laser is used for dopant activation with a wavelength of 248 nm and a <30 ns pulse width. A 0.36 J/cm² laser energy density is used to reach a low sheet resistivity for ion-implanted source–drain Si interfaces are important for low C–V roll-off [15].

To study the Vfb shift mechanism, we also used Fluorine (F) ion implantation into Si channel at a dosage of 1 × 10¹⁴ cm⁻² and energy of 10 keV. Alternatively, low temperature silicide-induced doping for source–drain of metal-gate/high-κ CMOS was also fabricated to decrease the interface reaction. After gate patterning, self-aligned 20 nm or Sb 5 nm Ga and thin Ni were deposited for respective n- and p-MOSFET, followed by silicide-induced doping at 600–650 °C RTA and removing the non-reacted metals [14]. The fabricated MOSFETs were characterized by capacitance–voltage (C–V) and current–density–voltage (J–V) measurements.

3. Results and discussion

3.1. Interface reaction and Vfb roll-off at thinner EOT

Fig. 1 shows the schematic diagram of a metal-gate/high-κ MOSFET, where both top metal-gate/high-κ and bottom high-κ/Si interfaces are important for low Vt CMOS as discussed following.

![Schematic MOSFET diagram with metal-gate, high-κ and interfaces.](image)

Fig. 1. Schematic MOSFET diagram with metal-gate, high-κ and interfaces.

Fig. 2. C–V characteristics of mixed high-κ HfLaON n- and p-MOS capacitors with various metal-gates after 1000 °C RTA.

![C–V characteristics of mixed high-κ HfLaON n- and p-MOS capacitors with various metal-gates after 1000 °C RTA.](image)

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Fig. 2. C–V characteristics of mixed high-κ HfLaON n- and p-MOS capacitors with various metal-gates after 1000 °C RTA. The adding La₂O₃ into HfO₂ with nitridation can achieve wanted negative Vfb in TaN/HfLaON n-MOS at 1.6 nm EOT, while needed positive Vfb is also reachable using high work-function Ir₃Si gate on HfLaON, even after 1000 °C RTA. These results indicate the good Vfb control for n- and p-MOS in top metal-gate/high-κ interface. The nitridation is important for HfLaON to preserve an amorphous structure at 1000 °C RTA, where the HfLaO starts to crystallize at RTA temperature above 900 °C RTA [10].

However, as the EOT of HfLaON gate dielectric scaled down to 1.2 nm, severe Vfb roll-off was found using the same Ir₃Si metal-gate. Although negative Vfb was still obtained for n-MOS using lower work-function HfSi₂-x gate, no proper work-function metal-gate can be used for p-MOS under the requirement of 1000 °C RTA for process integration. To analyze the Vfb roll-off effect from 1.6 nm to 1.2 nm EOT, we have examined the Vfb dependence. The Vfb is related to the fixed oxide charges (Qf), distributed oxide charges (ρox(x)), work-function difference between metal-gate and Si (φms – φm – φs), and Vf:

\[ V_f = \frac{Q_f}{C_{ox}} + \frac{1}{C_{ox}} \int_0^{EOT} x \rho_{ox}(x) dx \]  

(1)

\[ V_f = V_f + 2\phi_f + Q_{dep}/C_{ox} \]  

(2)

Here Cox is the gate capacitance, Q_{dep} is the depletion charge and 2ϕf is the surface potential bending at onset of charge inversion. Since the same Ir₃Si/HfLaON gate stack and 1000 °C thermal cycle were used, the Vfb roll-off at thinner EOT is unlikely from the top metal/high-κ interface or φm difference. The ϕf, ϕs and Q_{dep} depend strongly on the doping concentration of Si, which is also kept the same when scaling down the EOT. Therefore, the Vfb roll-off at thinner EOT is due to oxide charges and/or dipoles [11] from the above equation.

Here we propose that the oxide charges at thinner EOT are generated from interface reaction at high temperature:

\[
\text{Si} + \text{HfO}_2 \rightarrow \text{SiO}_x + \text{HfO}_{2-x} \]  

(3)

Such interface reaction, generating oxygen vacancy charges of non-stoichiometric SiOx and HfO₂₋ₓ, is inevitable at 1000 °C RTA due to the close bond enthalpy of SiO₂ (800 kJ/mol) and HfO₂ (802 kJ/mol) [9]. Here the bond enthalpy is defined as the standard molar enthalpy change of bond dissociation that generates fragments in the gaseous state at 298 K and a pressure of 100 kPa. From the interface reaction and Vfb roll-off effect at thinner EOT, the bottom high-κ/Si interface is also the key factor for low Vf CMOS.

3.2. Solution 1 – inserting an interfacial oxide

One method to lower interface reaction is to insert a thin oxide. Fig. 3a shows the C–V characteristics of MoN/HfAlO/SiON p-MOS capacitors. Using both unique positive Vfb of Al₂O₃ in HfAlO and high work-function metal-gate of MoN, this gate stack can reach the needed positive Vfb. Besides, a small EOT of 0.85 nm is also obtained from quantum-mechanical C–V calculation with 10⁴ times better leakage current than SiO₂. To further understand the reached small EOT even by inserting a SiON, we have used Secondary Ion Mass Spectroscopy (SIMS) to exam the MoN/HfAlO/SiON gate stack. As shown in Fig. 3b, the achieved small EOT with an interfacial SiON is due to the controlled diffusion of both Al and Mo into SiON, where various thick SiON were used to optimize the EOT and interface reaction.

Although the detailed mechanism of the unique positive Vfb shift in Al₂O₃ is still under study, it may be related to the generation of charged oxygen vacancies predicted theoretically [18]. Such charged oxygen vacancies in Al₂O₃ is related to the lower bond
enthalpy of Al–O bond (511 kJ/mol) and Si–N bond (470 kJ/mol) in SiON than that of Si–O bond and Hf–O bond [9]. We have designed an experiment using F+ channel ion implantation to examine this charged oxygen vacancy model. The measured C–V characteristics of the same MoN/HfAlO/SiON gate capacitor, with F+ channel ion implantation, is also shown in Fig. 3a for comparison. Both the Vfb shift and capacitance density are degraded in F+ implanted samples. Since F-atom has the largest electronegativity, the Vfb shift can be blocked by ion-implanted F-atoms with bonding to oxygen vacancies in Al2O3. This may further degrade the capacitance density due to the formation lower-j SiOF in HfAlO gate dielectric. Here the SiOF is a well known low-j dielectric for backend isolation with j value lower than SiO2.

3.3. Solution 2 – laser-reflective-gate MOS structure

However, further scaling EOT using metal-gate/high-j/interfacial oxide gate stack may also run out of solution due to the lower-j interfacial SiON. Since the interface reaction in Eq. (3) follows the basic chemistry of Arrhenius temperature dependence, the low temperature process is another solution. We have developed a laser-reflective-gate MOS structure shown in inserted Fig. 4, which can decrease the laser energy absorption under the gate stack during laser annealing to activate the ion-implanted source–drain [15]. Fig. 4 shows the comparison of C–V characteristics of TaN/[Ir3Si–HfSi2–x]/HfLaON respective p- and n-MOSFETs with and without the top laser reflective Aluminum (Al) gate. Here the Al/TaN gate can achieve a high reflectivity as much as 91% for 248 nm KrF excimer laser in a reflectivity measurement, but the TaN gate only reflects 36% at the same condition. From the measured C–V characteristics, the Vfb roll-off is suppressed for Al/TaN/[Ir3Si–HfSi2–x]/HfLaON p- and n-MOS capacitors compared with the similar devices without top Al laser-reflective layer, under the same laser annealing condition of 0.36 J/cm² laser fluence. This large improvement is due to the preserved low temperature at high-k/Si interface by laser-reflective-gate CMOS design, during source–drain dopant activation by laser annealing. Besides, an EOT of 1.05 nm is obtained from quantum-mechanical C–V calculation.

The transistor I–V characteristics of Al/TaN/[Ir3Si–HfSi2–x]/HfLaON CMOSFETs are shown in Fig. 5. In addition to the good device characteristics, low Vt of 0.16 and 0.13 V were obtained for Al/TaN/[Ir3Si–HfSi2–x]/HfLaON p- and n-MOSFET, respectively, at a small 1.05 nm EOT. Besides, this laser-reflected-gate metal-gate/high-k CMOS has the merits of simple gate-first and self-aligned process. The achieved low Vt using laser-reflective-gate structure further supports the proposed interface reaction model.

3.4. Solution 3 – silicide-induced doping for source–drain shallow junction

To further investigate our proposed Vfb roll-off effect by interface reaction, we have measured C–V characteristics of TaN/LaTiO p-MOS capacitors under different RTA temperature. The TiO con-
MOS capacitors. Support that the interfacial oxide layer from the TEM analysis. These results increasing RTA temperature. The degraded EOT is due to the form-

600 to 900 °C.

concentration in LaTiO is 25% by the calibrated thickness rate of TiO2 and La2O3 during LaTiO deposition by PVD. As shown in Fig. 6, the Vb roll-off increases with increasing RTA temperature from 600 to 900 °C. In addition, a degraded EOT is also found with increasing RTA temperature. The degraded EOT due to the forming interfacial oxide layer from the TEM analysis. These results support that the Vb roll-off effect is strongly related to the interface reaction. Besides, the Vb roll-off effect can also be decreased by decreasing process temperature.

Using the low temperature process of 600–650 °C and work-function tuning of TaN and Ir gate metals, we have fabricated the [TaN–TaN/Ir]/LaTiO n- and p-MOS capacitors, respectively. As shown in the C–V characteristics of Fig. 7, proper negative and positive Vb values are still obtained even at small EOT of 0.59 and 0.66 nm for n- and p-MOS capacitors, respectively. The different EOT value between n- and p-MOS devices is due to the different electron and hole effective mass and wave-function distribution, from quantum-mechanical C–V calculation. However, the challenge is how to fabricate the MOSFET at low temperature. Conventionally, a high temperature RTA of 1000 °C is required to activate ion-implanted dopants in the source–drain of a MOSFET. The other methods to dope the source–drain at low temperature are the solid-phase diffusion and silicide-induced doping [14]. Here we used silicide-induced doping to fabricate the CMOS devices since it has even lower process temperature than using solid-phase diffusion. Fig. 8 shows the Id–Vg characteristics of self-aligned and gate-first LaTiO n- and p-MOSFETs with low temperature NiSi-induced source–drain dopants.

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4. Conclusions

We have analyzed the Vb roll-off effect at smaller EOT and proposed a mechanism of charged oxygen vacancies by interface reaction for the explanation. To decrease the interface reaction, a thin SiON was inserted in high-κ/Si. The needed positive Vb and a small 0.85 nm EOT are achieved in MoN/HfAlO/SiON p-MOS. The interface reaction can also be decreased by using novel low temperature process from its Arrhenius temperature dependence. Using laser-reflective-gate MOS design to preserve low temperature under the gate stack, low Vt of −0.16 and 0.13 V were obtained for Al/TaN/Ir3Si–HfSi2-p/HfLaON p- and n-MOSFET, respectively, at a small 1.05 nm EOT. Using the low temperature NiSi-induced doping in source–drain instead of conventional ion-implantation and 1000 °C RTA, low Vt of −0.17 and 0.21 V were reached at respective 0.66 and 0.59 nm EOT.

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